CLAIMS

What is claimed is:

1. A magnetic tunnel junction memory cell comprising:

a non-linear element;

a first electrically conductive line coupled to the non-linear element;

a second electrically conductive line overlapping the first conductive line at a first intersection region;

means for conducting magnetic flux wherein the means for conducting magnetic flux are positioned at the first intersection region in a vertical space between the first conductive line and the second conductive line;

a magnetic tunnel junction memory element sandwiched by the means for conducting magnetic flux and electrically connected in series with the second conductive line, the means for conducting magnetic flux and the non-linear element;

a third electrically conductive line parallel to the first conductive line; and

a fourth electrically conductive line parallel to the second conductive line, overlapping the third conductive line at a second intersection region and defining a corner at the second intersection region, wherein the means for conducting magnetic flux are positioned in the corner at the second intersection region.

2. The magnetic tunnel junction memory cell of claim 1 wherein the means for conducting magnetic flux comprising at least a bottom magnetic portion and a top magnetic portion with the memory element being sandwiched between the top magnetic portion and the top magnetic portion.

3. The magnetic tunnel junction memory cell of claim 1, further including a first non-magnetic electrically conductive spacer and a second non-magnetic electrically conductive spacer, wherein the first non-magnetic spacer and the second non-magnetic

spacer are positioned on either sides of the magnetic tunnel junction memory element to magnetically separate the magnetic tunnel junction memory element from the means for conducting magnetic flux.

4. The magnetic tunnel junction memory cell of claim 1 wherein the magnetic tunnel junction memory element comprising:

a first magnetic layer comprising a perpendicular magnetization film;

a second magnetic layer comprising a perpendicular magnetization film having a higher coercive force than that of the first magnetic layer; and

a tunnel barrier layer sandwiched between the first magnetic layer and the second magnetic layer.

5. The magnetic tunnel junction memory cell of claim 4, further including a plurality of spin-polarizing layers positioned at least on one side of the tunnel barrier layer between the tunnel barrier layer and one of the magnetic layers.

6. A magnetic tunnel junction memory cell comprising:

a non-linear element;

a first electrically conductive read line coupled to the non-linear element;

a second electrically conductive read line wherein the first read line and the second read line are preferably orthogonal and overlap each other at a read intersection region;

a first electrically conductive write line being parallel to the first conductive read line;

a second electrically conductive write line being parallel to the second conductive read line, wherein the first conductive write line and the second conductive write line overlap each other at a write intersection region and define a write corner;

a magnetic flux guide comprising a first end and a second end, and being positioned at the read intersection region in the write corner; and

a magnetic tunnel junction memory element positioned between the second end of the magnetic flux guide and the second read line, wherein the memory element is electrically connected in series with the second conductive read line, the magnetic flux guide and the non-linear element.

7. The magnetic tunnel junction memory cell of claim 6 wherein the second conductive read line has a multilayer structure comprising at least one conductive magnetic layer with the conductive magnetic layer being positioned adjacent the magnetic tunnel junction memory element.

8. The magnetic tunnel junction memory cell of claim 6 wherein the magnetic tunnel junction memory element comprises:

a first magnetic layer having a perpendicular magnetization;

a second magnetic layer having a perpendicular magnetization and a coercive force higher than that of the first magnetic layer; and

a tunnel barrier layer sandwiched between the first magnetic layer and the second magnetic layer.

9. The magnetic tunnel junction memory cell of claim 8, further including a first electrically conductive non-magnetic spacer and a second electrically conductive non-magnetic spacer positioned on either side of the memory element to magnetically isolate the memory element from the magnetic flux guide and the second read line, wherein the first non-magnetic spacer is positioned at the first magnetic layer and at a second non-magnetic spacer is positioned at the second magnetic layer.

10. The MTJ memory cell of claim 9 wherein the second non-magnetic spacer having a direct contact with the second magnetic layer can be made of an antiferromagnetic material to stabilize a domain structure of the second magnetic layer.

11. A nonvolatile memory array comprising:

a substrate;

a first plurality of electrically conductive lines formed on the substrate;

a second plurality of electrically conductive lines formed on the substrate and overlapping the first plurality of the lines at a plurality of first intersection regions;

a plurality of memory cells formed on the substrate, each memory cell being positioned at a first intersection region between one of the first plurality of lines and one of the second plurality of lines, each memory cell comprising a non-linear element, a magnetic flux guide and a magnetic tunnel junction memory element electrically connected in series with one another and with one of the second plurality of conductive lines, wherein one of the first plurality of conductive lines is coupled to the non-linear element;

a third plurality of electrically conductive lines formed on the substrate, being parallel to the first plurality of lines and being positioned in a vertical space between the first plurality of lines and the second plurality of lines; and

a fourth plurality of electrically conductive lines formed on the substrate, being parallel to the second plurality of lines, being positioned in the vertical space between the first plurality of lines and the second plurality of lines, overlapping the third plurality of lines at a second plurality of intersection regions and defining a plurality of corners.

12. The nonvolatile memory array of claim 11, further including a first write circuitry coupled to the third plurality of lines and a second write circuitry coupled to the fourth plurality of lines, whereby during a write operation a current simultaneously passing through one of the third plurality of lines and one the fourth plurality of lines at one of the plurality of corners generates a magnetic filed acting on the magnetic tunnel junction memory element through the magnetic flux guide.

13. The nonvolatile memory array of claim 11, further including a first read circuitry coupled to the first plurality of lines and a second read circuitry coupled to the

second plurality of lines for detecting a tunnel current through the magnetic tunnel junction memory element in a direction perpendicular to the substrate when a voltage across the non-linear element is greater than a threshold voltage of the non-linear element.

14. The nonvolatile memory array of claim 11 wherein the magnetic tunnel junction memory elements comprising:

a tunnel barrier layer having a major plane;

a first magnetic layer having a magnetization oriented perpendicular to the major plane of the tunnel barrier layer; and

a second magnetic layer having a magnetization oriented perpendicular to the major plane of the tunnel barrier layer, wherein a coercive force of the second magnetic layer is higher than that of the first magnetic layer, and wherein the tunnel barrier layer is sandwiched between the first magnetic layer and the second magnetic layer.

15. The nonvolatile memory array of claim 11, further including a plurality of electrically conductive non-magnetic spacers, positioned on either side of the memory element to magnetically isolate the memory element from the magnetic flux guide.

16. The nonvolatile memory array of claim 11 wherein the magnetic flux guide comprises a magnetic pad, a magnetic stud and a magnetic cap.

17. The nonvolatile memory array of claim 16 wherein the magnetic cap and the magnetic pad overhang the magnetic stud and, one of the third plurality of lines and one of the fourth plurality of lines at one of the plurality of corners.

18. The nonvolatile memory array of claim 16 wherein the magnetic pads and the magnetic caps of the plurality of memory cells are magnetically isolated from one another by a plurality of non-magnetic gaps.

19. A method of operating a magnetic tunnel junction memory cell comprising:

generating a magnetic write flux by passing a write current through an electrically conductive write line and an electrically conductive excitation line overlapping the write line and defining a corner;

orienting a first magnetization orientation in a free magnetic layer of a magnetic tunnel junction memory element perpendicular to a major plane of a tunnel barrier layer using the magnetic write flux conducted through a magnetic flux guide, wherein the magnetic flux guide is positioned in the corner and comprises a first magnetic portion and a second magnetic portion, and the memory element is sandwiched between the first magnetic portion and the second magnetic portion of the magnetic flux guide; and

sensing the first magnetization orientation in the free magnetic layer by passing a sense current through the memory element between an electrically conductive bit line and an electrically conductive word line in a direction generally perpendicular to the major plane of the tunnel barrier layer and by detecting a resistance of the memory element, wherein the memory element comprises the tunnel barrier layer, the free magnetic layer and a pinned magnetic layer with the tunnel barrier layer being sandwiched between the pinned magnetic layer and the free magnetic layer;

whereby the resistance of the memory element is determined by the first magnetization orientation in the free magnetic layer relative to a second magnetization orientation in the pinned magnetic layer having a coercive force higher than that of the free magnetic layer, wherein the second magnetization orientation is perpendicular to the major plane of the tunnel barrier layer.

20. The method of operating the magnetic tunnel junction memory cell of claim 19, further including spin-polarizing the sense current with a first spin-polarizing layer and with a second spin-polarizing layer, wherein the first spin-polarizing layer is positioned

between the pinned magnetic layer and the tunnel barrier layer and the second spin-polarizing layer is positioned between the free magnetic layer and the tunnel barrier layer.

21. The method of operating the magnetic tunnel junction memory cell of claim 19 further including stabilizing a domain structure of the pinned magnetic layer by an exchange coupling with an anti-ferromagnetic layer positioned between the pinned magnetic layer and the first portion of the magnetic flux guide.

22. A method of operating of a magnetic tunnel junction memory cell comprising:

generating a magnetic write flux by passing a write current through a first electrically conductive line and a second electrically conductive line, wherein the second conductive line overlaps the first conductive line and defines a corner;

orienting a first magnetization orientation in a pinned magnetic layer of a magnetic tunnel junction memory element perpendicular to a major plane of a tunnel barrier layer using the magnetic write flux conducted through a magnetic flux guide, wherein the magnetic flux guide is positioned in the corner and comprises a first magnetic portion and a second magnetic portion, and the memory element is positioned between the first portion and the second portion of the magnetic flux guide; and

sensing the first magnetization orientation in the pinned magnetic layer by passing a sense current through the tunnel barrier layer in a direction generally perpendicular to the major plane of the tunnel barrier layer and by detecting a resistance of the memory element, wherein the magnetic tunnel junction element comprises the pinned magnetic layer and a free magnetic layer sandwiching the tunnel barrier layer;

whereby the resistance of the memory element is determined by the first magnetization orientation in the pinned magnetic layer relative to a second magnetization orientation in the free magnetic layer having a coercive force lower than that of the pinned magnetic layer when the sense current flows through the tunnel barrier layer; a magnetic state of the memory

element is determined by the first magnetization orientation in the pinned magnetic layer.

23. The method of operating of the magnetic tunnel junction memory cell of claim 22 wherein sensing the first magnetization orientation in the pinned magnetic layer includes:

generating a magnetic excitation flux by passing an excitation current of a predetermined polarity and of a predetermined strength through a second electrically conductive line;

applying the magnetic excitation to the memory element through the magnetic flux guide to orient the second magnetization orientation in the free layer perpendicular to the major plane of the tunnel barrier layer in a predetermined direction; and

sensing the magnetic state of the memory element by passing the sense current through the magnetic tunnel junction memory element between a third electrically conductive line and a fourth electrically conductive line, wherein the third conductive line is orthogonal to the fourth conductive line, overlaps the fourth conductive line at an intersection region, and the memory element is positioned in a vertical space between the third conductive line and the fourth conductive line at the intersection region.